AutoPNN
Automated Printed Neural Network Design

Georgios Zervakis
University of Patras, Patras, Greece
zervakis@ceid.upatras.gr

***Abstract*—Printed and flexible electronics offer a promising path toward enabling mechanically flexible and sustainable domain-specific processing elements, paving the way for a new class of applications at the extreme far edge. Although the market for printed and flexible electronics is rapidly expanding, the technology still faces significant limitations, notably its low integration density. This limitation casts doubt on the feasibility of implementing printed classifiers, which are often essential for such applications. Several unconventional design approaches have been adopted to reduce hardware overheads and improve feasibility; however, they come at the cost of increased design complexity. Therefore, design automation techniques for domain-specific printed classifiers are essential to overcome these technological barriers and to support broader adoption and commercialization.**

***Index Terms*—Design Automation, Neural Networks, Printed Electronics**

I. Introduction

Printed and flexible electronics refer to integrated circuits built on substrates that can stretch, bend, roll, and conform to surfaces. Printed and flexible electronics offer exceptional advantages in cost and form factor. Silicon manufacturing imposes significant operational, testing, and compliance costs. In contrast, printed and flexible circuits can be fabricated in smaller distributed facilities, with cheaper and even portable equipment, without the need for protective packaging, while a key feature of such technologies is sustainability [1].

Their lightweight and thin profiles, combined with their flexibility and extremely low cost, enable the integration of innovative services in a vast number of far-edge applications that have witnessed limited computing infiltration. Such applications include smart packaging, disposables, forensics, and accessible healthcare products and wearables [1]–[3].

II. Design Challenges

Despite their appealing characteristics, printed electronics come with large feature size and elevated device latency and power consumption rendering the realization of complex circuits–such as machine learning classifiers that are oftenly required in targeted applications–extremely challenging. To address these extreme hardware overheads, unconventional approaches such as bespoke design and approximate computing have emerged as the de facto design solution for printed classifiers [1]. Although remarkable area gains can be achieved, such approaches increase design complexity by exploding the design space, which is heavily influenced by customization parameters, area efficiency, and approximation error. As a result, automating the design of printed classifiers–especially for neural networks–emerges as a key research challenge to align short fabrication timelines with equally short design cycles, ultimately reducing design costs and providing the necessary support for broader technology adoption.

III. Methods

A growing body of research has recently emerged toward automating the generation of printed neural networks. The authors of [2] were the first to recognize that the area of bespoke classifiers is highly dependent on the values of their trainable parameters, and they proposed approximating these parameters in a hardware-aware manner. Several subsequent works have built on this insight, offering varying area-accuracy trade-offs [3]–[6]. A common theme among them is the automated transition from dataset to Verilog within minutes. Interestingly, [7] observed that these techniques were so effective in reducing the immense area overhead of the classifiers that the mandatory analog-to-digital converters (ADCs), required for processing sensor data, became the actual bottleneck. This realization led the authors of [7] to propose an in-training co-design framework that, in addition to the classifier, also approximates the ADC circuit–significantly reducing the overall cost of the sensor–interfacing–classifier. Notably, to support their core mission, [2]–[7] have been made available open-source.

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