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Late Breaking Results: Energy-Efficient Printed Machine Learning Classifiers with Sequential SVMs

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***Abstract*—Printed Electronics (PE) provide a mechanically flexible and cost-effective solution for machine learning (ML) circuits, compared to silicon-based technologies. However, due to large feature sizes, printed classifiers are limited by high power, area, and energy overheads, which restricts the realization of battery-powered systems. In this work, we design sequential printed bespoke Support Vector Machine (SVM) circuits that adhere to the power constraints of existing printed batteries while minimizing energy consumption, thereby boosting battery life. Our results show 6.5x energy savings while maintaining higher accuracy compared to the state of the art.**

***Index Terms*—Machine Learning, Support Vector Machines, Printed Electronics**

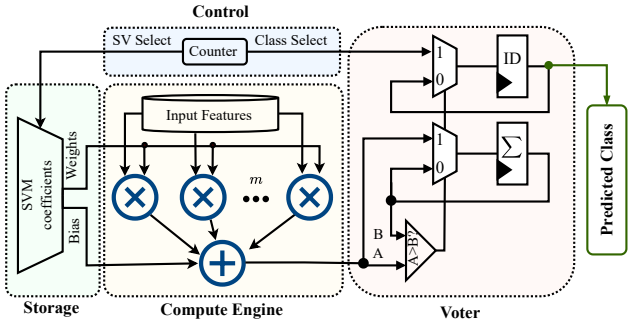

Fig. 1. Abstract overview of our proposed sequential SVM circuit design.

I. Introduction

Printed Electronics (PE) have emerged as a transformative technology designed to address the limitations of traditional silicon-based systems [1]. Printed devices offer mechanical flexibility, conformality, non-toxicity and ultra-low manufacturing and Non-Recurring Engineering (NRE) costs. However, PE come with large feature sizes, leading to strict power and area constraints, thus making the realization of complex datapaths–such as Machine Learning (ML) algorithms–challenging. Leveraging the low NRE and fabrication costs of PE, unconventional computing paradigms such as bespoke (i.e., fully customized circuits with hardwired values), and approximate computing have been exploited towards the realization of battery-powered printed ML circuits [2]–[4]. However, the state of the art mainly targets reducing area overheads, neglecting energy efficiency, which is crucial for extending battery life in printed applications.

In this work, we address these limitations and propose a ML classifier design that combines state-of-the-art accuracy with utmost energy efficiency. We focus on Support Vector Machines (SVMs) due to their effectiveness in classification tasks relevant to PE applications, and design sequential printed SVMs that compute one support vector per cycle, compressing the required compute engine and minimizing energy requirements. Moreover, the One-vs-Rest (OvR) algorithm is selected to minimize hardware requirements associated with support vectors storage. Our SVMs achieve $6.5\times$ average energy reduction compared to state-of-the-art approaches while achieving higher accuracy.

II. Proposed Printed Sequential SVMs

Algorithmic Implementation: SVMs are supervised learning algorithms that classify data by identifying an optimal hyperplane in a high-dimensional space. Effective for small, high-dimensional datasets, they are robust against overfitting by focusing on critical data points (i.e., support vectors) which define decision boundaries, based on which a series of classifiers can determine the predicted class. We employ linear kernels in our SVMs, due to their simplicity and reduced hardware complexity. Any linear classifier with m weights (w_i) and bias b computes the following weighted sum: $y = \sum_{i=1}^{m} w_i x_i + b$, where x_i are the input activations. Targeting multi-class classification, SVMs are built upon two mainstream algorithms: One-vs-One (OvO) and OvR. OvO creates $\frac{n(n-1)}{2}$ binary classifiers (for n classes), each trained to distinguish between a specific pair of classes. In contrast, n classifiers are required in OvR for separating each class from all others. Since OvR needs fewer support vectors, it is used in our implementation, targeting reduced hardware overheads. We train our SVMs with low-precision inputs and post-training, we quantize the SVM weights and biases to the lowest precision that can retain acceptable accuracy.

Hardware Implementation: We implement our trained SVMs as sequential architectures, targeting high energy efficiency alongside low area and power consumption. An overview of our proposed sequential SVM circuits is presented in Fig. 1. They comprise four major components: control, storage, compute engine, and voter. Orchestrated by our control circuitry, the classification output is produced over multiple cycles, aggregating to n total. In each cycle, a selected support vector is fetched from storage, for its associated weighted sum to be calculated by our compute engine. A $\log_2(n)$-bit counter is employed for control, responsible for accessing the stored support vectors and terminating the multi-cycle process once all classifiers have been computed. We opt for bespoke Multiplexer (MUX)-based storage units, i.e., the inputs of the MUX (excluding the control signal) are hardwired to the parameters of the support vectors. This is made feasible by

the low costs in PE. We also evaluated a crossbar-based Read-Only Memory (ROM) alternative [1]; however for the required storage size, crossbars prove more costly, mainly due to the need for printed Analog-to-Digital Converters (ADCs). The control counter produces the select signal of the MUX. The above showcase the two-fold advantage of using the OvR algorithm: compared to OvO, which is used in the state of the art, fewer support vectors need to be stored, and less complicated control signals are needed, thus minimizing overheads at both the control and storage components. The entire SVM computation is folded over one compute engine, which computes the weighted sum for each support vector fetched from the MUX. Our engine instantiates m multipliers and a multi-operand adder, thus computing one classifier per cycle and significantly reducing the hardware resources compared to fully parallel architectures [2], [3], where dedicated hardware per coefficient is required. The output of our compute engine is sent to our voter, which tracks the classifier (i.e., counter value) with the highest score (i.e., weighted sum). Hence, our voter–essentially a sequential `argmax`–requires only two registers (for score and classifier id) and a single comparator, as finding the maximum score involves one comparison per cycle between the current and stored scores.

III. Evaluation & Results

Experimental Setup: We evaluate our printed sequential SVMs over five datasets from the UCI ML repository [5]. Synopsys Design Compiler and PrimeTime are used for hardware evaluation with the EGFET PDK [1], targeting frequency in the Hz range, typical for printed applications [1]. Our SVMs are trained with normalized inputs to $[0, 1]$ and a random $80\%/20\%$ split for training/testing data subsets. Accuracy is reported on the test dataset. For comparisons, we consider the printed fully-parallel SVMs [2], [3] and Multi-Layer Perceptrons (MLPs) [4], since they achieve high accuracy.

Results: Table I presents the results of our comparison against the state of the art, in terms of accuracy area, power, frequency, latency and energy. Overall, our sequential SVMs feature the most favorable accuracy-energy trade-off among related approaches. Across all datasets, we achieve higher accuracy by 2.02%, 3.13%, and 4.38% on average, compared to each state-of-the-art technique [2], [3], and [4], respectively. An exception can be found for the PenDigits dataset, where the state of the art employs a larger number of support vectors to retain accuracy, but incurs unrealistic hardware overheads.. Our SVMs, despite showing small area overheads in some cases, compared to related works, manage to stay within acceptable area ranges, satisfying the constraints of typical printed applications [3]. Additionally, our peak power consumption is $22.9\,\mathrm{mW}$ and the average $13.58\,\mathrm{mW}$, which enables *all* our designs to be powered by existing printed batteries (e.g., Molex $30\,\mathrm{mW}$). In contrast, only 4 designs of the state of the art can be powered by an existing printed power source. Importantly, our circuits achieve an average energy consumption of only $2.46\,\mathrm{mJ}$, which corresponds to a $10.6\times$ improvement over [2], $5.4\times$ over [3], and $3.46\times$ over [4]. Our circuits feature the best energy consumption in all but one dataset (RedWine), where the difference is only $0.17\,\mathrm{mJ}$, but our accuracy is significantly better in that case (8% higher). With an average energy improvement of $6.5\times$, our SVMs can successfully boost battery life in printed applications.

TABLE I
Hardware evaluation of our proposed sequential SVMs and comparison with state-of-the-art techniques [2]–[4].

Dataset†	Model	Acc. (%)	Area (cm^2)	Power (mW)	Freq. (Hz)	Latency (ms)	Energy (mJ)
Cardio	SVM [2]	90.0	15.1	57.4	13	75	4.31
Cardio	SVM [3]⋆	89.0	17.0	48.9	13	75	3.67
Cardio	MLP [4]⋆	87.0	6.1	20.8	5	200	4.16
Cardio	***Ours***	93.4	17.1	17.6	38	78	1.373
Derm.	SVM [2]	97.2	60.4	182.9	8	120	21.95
Derm.	***Ours***	98.6	13.9	14.3	38	156	2.231
PD	SVM [2]	97.8	123.8	364.4	4	250	91.1
PD	SVM [3]⋆	97.0	97.0	183.7	4	250	45.92
PD	MLP [4]⋆	93.0	32.7	99.2	4	250	24.8
PD	***Ours***	93.1	22.9	22.9	35	280	6.41
RW	SVM [2]	57.0	23.5	92.8	15	66	6.12
RW	SVM [3]⋆	56.0	11.7	21.3	15	66	1.41
RW	MLP [4]⋆	56.0	1.1	3.9	5	200	0.79
RW	***Ours***	64	6.2	6.7	42	144	0.965
WW	SVM [2]	53.0	28.3	112.4	17	60	6.74
WW	SVM [3]⋆	52.0	11.0	34.7	17	60	2.08
WW	MLP [4]⋆	53.0	6.5	21.3	5	200	4.26
WW	***Ours***	56	6	6.4	34	203	1.299

†Derm.: Dermatology, PD: PenDigits, RW: RedWine, WW: WhiteWine
⋆Approximate model.

IV. Conclusion

In this work, we propose highly-accurate and energy-efficient sequential SVMs, tailored for printed technology. Our bespoke designs utilize the OvR algorithm and perform classification over multiple cycles, limiting hardware overheads. Compared to parallel alternatives from the state of the art, our circuits deliver higher accuracy, with an energy improvement of $6.5\times$, whilst satisfying the stringent area and power constraints of PE. Thus, our proposed designs can be powered by existing printed batteries (e.g., Molex $30\,\mathrm{mW}$), and even prolong their battery lifetime in printed applications.

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